US005697086A

United States Patent [19]

Svoboda

[11] Patent Number: 5,697,086

[45] Date of Patent: Dec. 9, 1997

[54] **CO-CHANNEL FM SIGNAL/INTERFERENCE CANCELLER**

[75] Inventor: **Esteban O. Svoboda**, San Jose, Calif.

[73] Assignee: **GTE Government Systems Corporation**, Del.

[21] Appl. No.: **228,060**

[22] Filed: **Apr. 15, 1994**

[51] **Int. Cl.**[6] **H04B 1/10**

[52] **U.S. Cl.** **455/304**; 455/206; 455/260; 329/336; 329/316; 329/325

[58] **Field of Search** 455/304, 302, 455/303, 305, 306, 206, 260, 126, 214; 329/336, 327, 316, 320, 325

[56] **References Cited**

U.S. PATENT DOCUMENTS

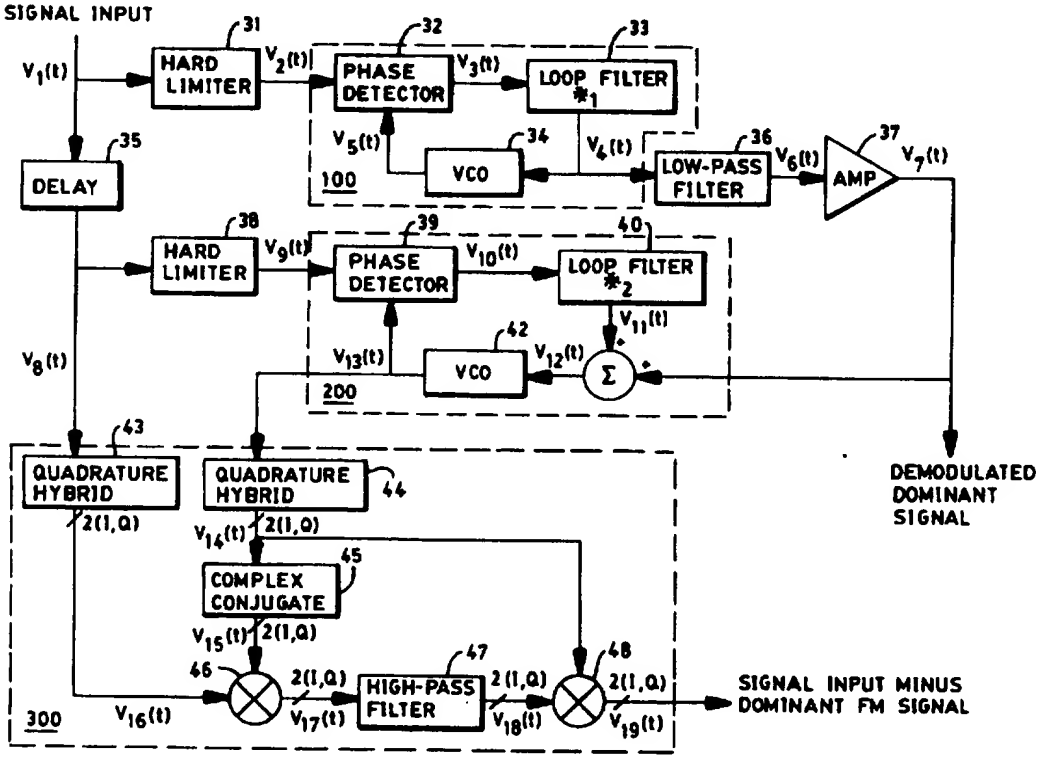
3,199,028	8/1965	Molin et al.	455/126 X
3,753,123	8/1973	Carpenter et al.	455/304
4,859,958	8/1989	Myers	455/206 X
4,992,747	2/1991	Myers	455/206 X
5,038,115	8/1991	Myers et al.	455/260 X

Primary Examiner—Reinhard J. Eisenzopf
Assistant Examiner—Philip J. Sobutka
Attorney, Agent, or Firm—James J. Cannon, Jr.; J. Stephen Yeo

[57] **ABSTRACT**

A combination of two phase-lock loops, and a cancellation circuit are used to remove a dominant FM signal from within a signal environment. The two phase-lock loops together produce a replica of the highest power (i.e. dominant) FM signal. The cancellation circuit uses this replica in a demodulation, notch-filtering, and remodulation process to excise the dominant FM signal, leaving the other signal(s) undisturbed. Potential applications include co-channel FM signal/interference cancellation and optimizing utilization of RF spectrum.

1 Claim, 3 Drawing Sheets



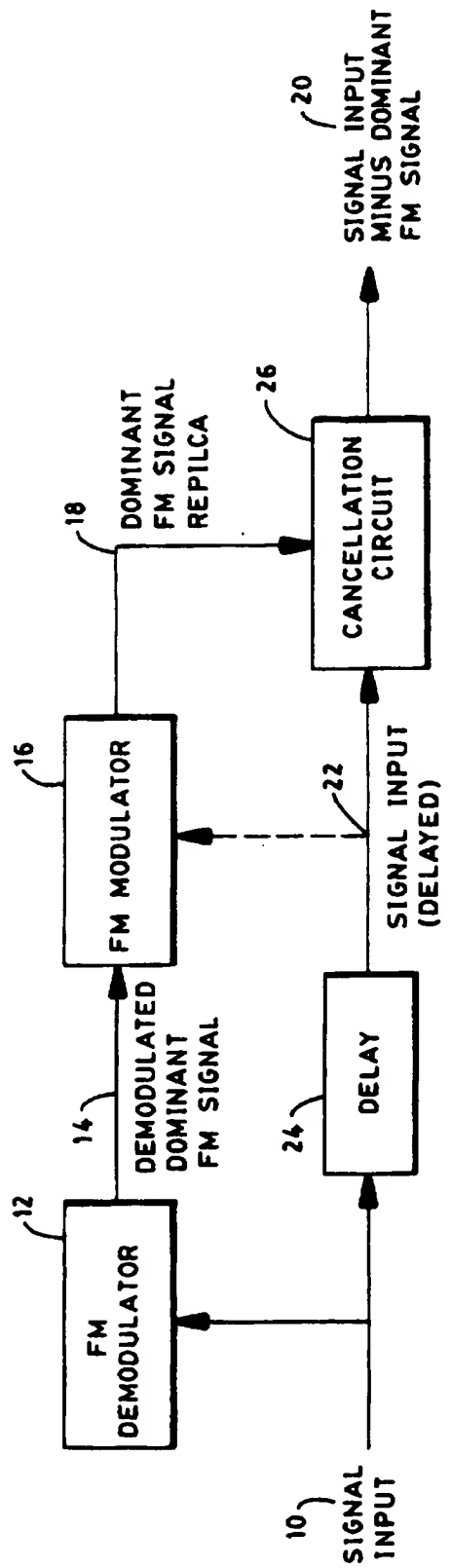

10
SIGNAL INPUT
12
FM DEMODULATOR
14
DEMODULATED DOMINANT FM SIGNAL
16
FM MODULATOR
18
DOMINANT FM SIGNAL REPILCA
20
SIGNAL INPUT MINUS DOMINANT FM SIGNAL
22
SIGNAL INPUT (DELAYED)
24
DELAY
26
CANCELLATION CIRCUIT

FIG. 1

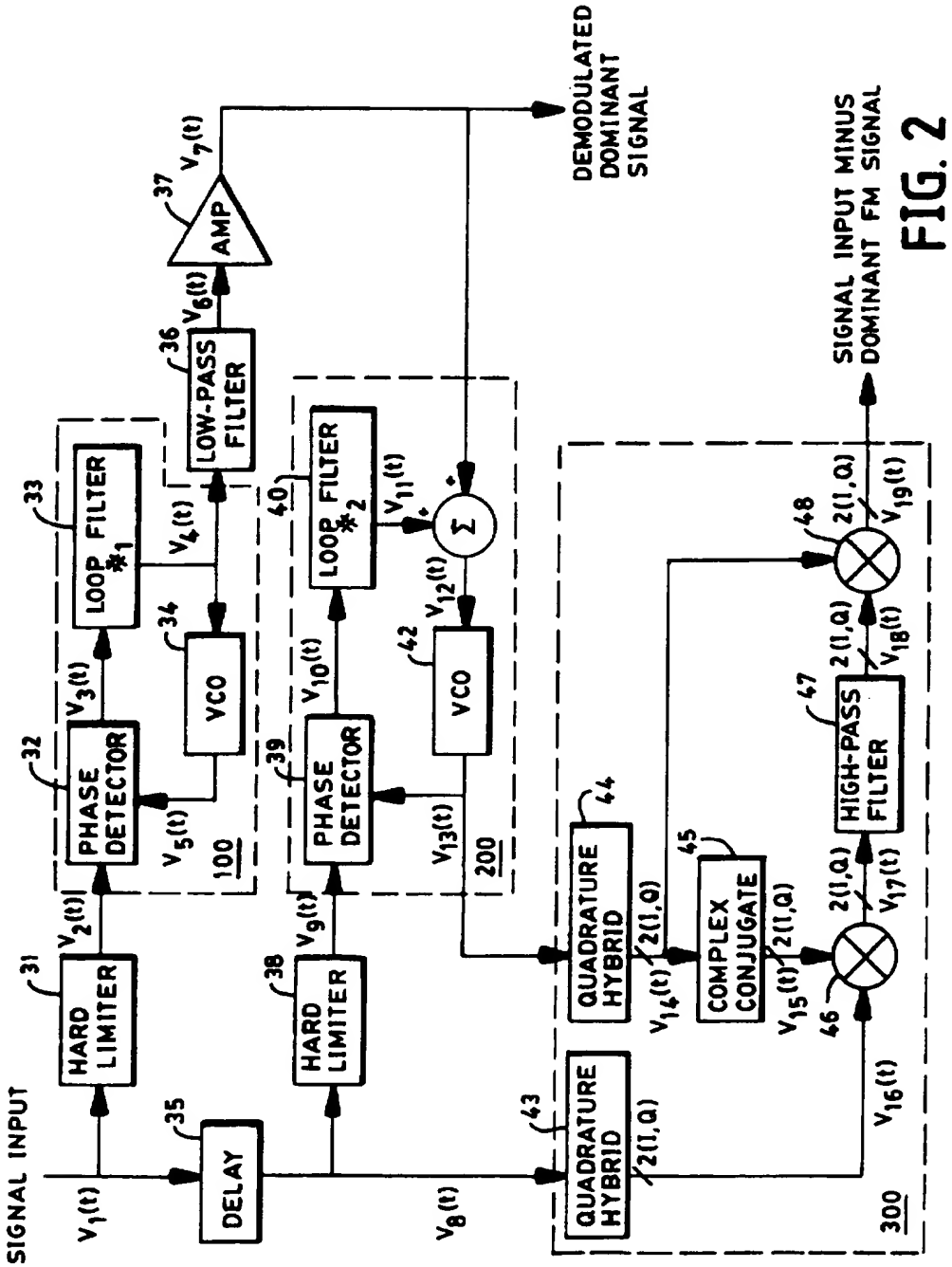

SIGNAL INPUT
$V_1(t)$
HARD LIMITER
31
$V_2(t)$
PHASE DETECTOR
32
$V_3(t)$
LOOP FILTER *1
33
$V_4(t)$
VCO
34
$V_5(t)$
100
DELAY
35
LOW-PASS FILTER
36
$V_6(t)$
AMP
37
$V_7(t)$
DEMODULATED DOMINANT SIGNAL
$V_8(t)$
$V_9(t)$
HARD LIMITER
38
$V_{10}(t)$
PHASE DETECTOR
39
$V_{11}(t)$
LOOP FILTER *2
40
$V_{12}(t)$
VCO
42
$V_{13}(t)$
200
QUADRATURE HYBRID
43
2(I,Q)
QUADRATURE HYBRID
44
$V_{14}(t)$
2(I,Q)
COMPLEX CONJUGATE
45
$V_{15}(t)$
2(I,Q)
46
$V_{16}(t)$
2(I,Q)
$V_{17}(t)$
HIGH-PASS FILTER
47
2(I,Q)
$V_{18}(t)$
2(I,Q)
48
$V_{19}(t)$
SIGNAL INPUT MINUS DOMINANT FM SIGNAL
300

FIG. 2

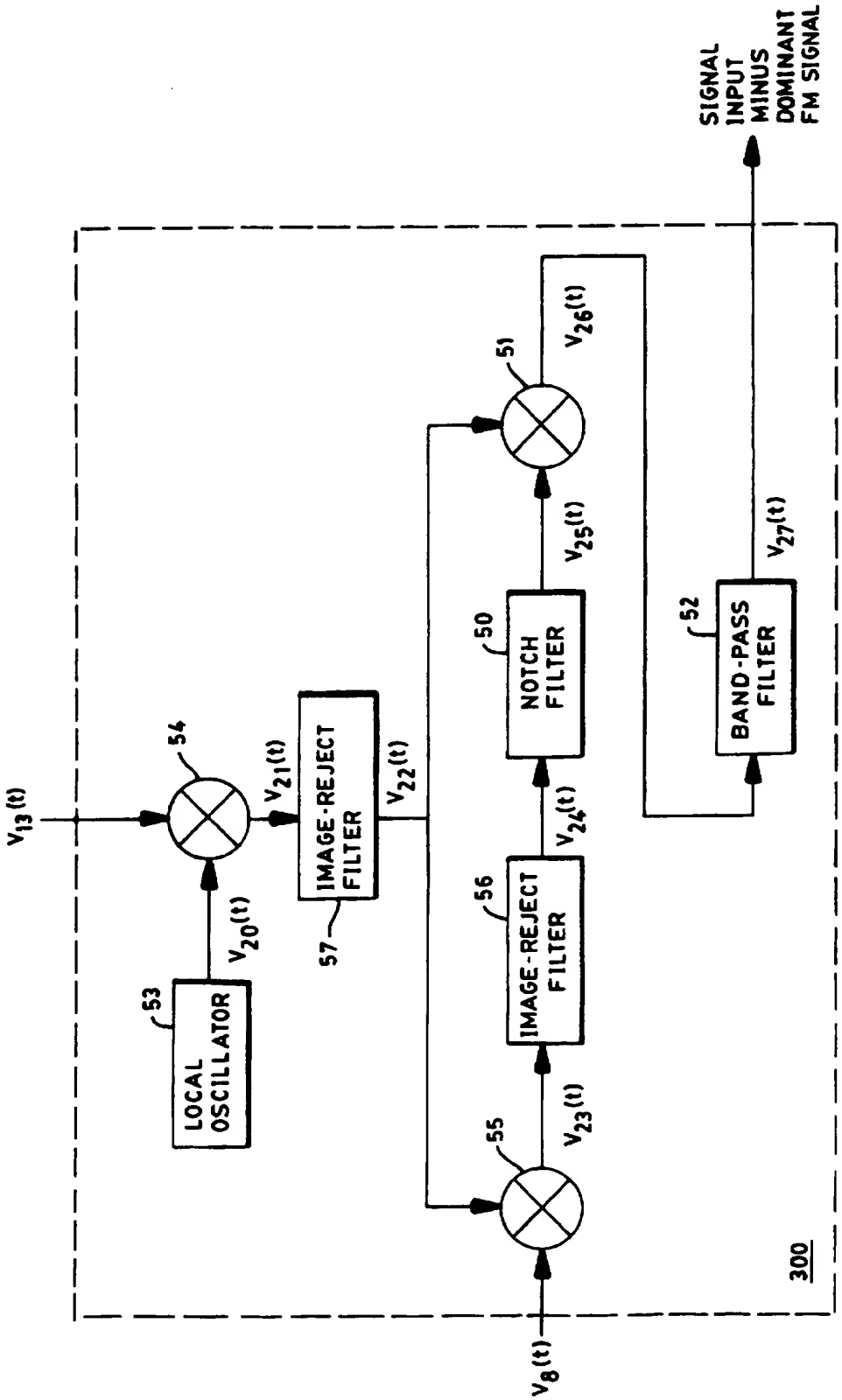

SIGNAL INPUT MINUS DOMINANT FM SIGNAL
$V_{13}(t)$
54
$V_{21}(t)$
IMAGE-REJECT FILTER
$V_{22}(t)$
57
$V_{20}(t)$
53
LOCAL OSCILLATOR
51
$V_{26}(t)$
$V_{25}(t)$
50
NOTCH FILTER
$V_{24}(t)$
56
IMAGE-REJECT FILTER
$V_{23}(t)$
55
$V_8(t)$
52
BAND-PASS FILTER
$V_{27}(t)$
300

FIG. 3

CO-CHANNEL FM SIGNAL/INTERFERENCE CANCELLER

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to radio signals and systems intended for removing the effects of co-channel FM signals and/or interference, or for increasing RF spectrum utilization.

2. Description of the Prior Art

The most relevant prior art for this invention are the disclosures of Myers et al. for which U.S. Pat. Nos. 4,859,958, 4,992,747 and 5,038,115 issued on Aug. 22, 1988, Feb. 12, 1991 and Aug. 6, 1991, respectively. In the last Myers et al. U.S. Pat. No. 5,038,115, two phase-lock loops were used to generate a 180° phase-shifted (i.e. inverted) replica of the dominant FM signal within a set of input signals, and this signal replica was subsequently added to the original set of signals to cancel out the dominant signal.

There are three practical problems associated with the last invention of Myers et al. First, the replica of the dominant signal produced by the two phase-lock loops will generally not match the original dominant signal with very high fidelity. Second, the additive cancellation process employed becomes ineffective when there are significant amplitude variations in the received dominant signal due to effects such as multipath and Rayleigh fading. Third, performance is adversely affected by phase shifts of the dominant signal replica that may result from DC drift in PLL components. The current invention solves these problems by improving upon the last invention of Myers et al. in three important ways, as disclosed herein.

The principal object of this invention is to provide an improved demodulator to excise a dominant FM signal, leaving the other signal(s) occupying the same frequency band undisturbed.

It is a further object of this invention to provide a novel combination of two phase-lock loops, and a cancellation circuit to separately demodulate multiple co-channel FM signals at different power levels.

SUMMARY OF THE INVENTION

The invention utilizes an FM demodulation means for recovering the modulating signal of a received dominant FM carrier signal, and an FM modulation means, using said modulating signal as input, for generating a replica of a received dominant FM carrier signal. A delay is provided for aligning in time the original signal input to the replica of the dominant FM signal. A cancellation circuit is provided for removing the dominant FM signal from the original set of input signals.

In a further aspect of the invention, the FM modulator includes a phase-lock loop with loop-bandwidth much narrower than the bandwidth of the signal modulating the dominant FM carrier and having as its VCO input the sum of its loop-filter output and the modulating signal of the dominant FM carrier.

In a still further aspect of the invention, the cancellation circuit includes a means for demodulating said dominant FM signal to a single spectral line at zero-frequency; a filter to notch out said spectral line, leaving the cross-products of all the original underlying signals and the complex-conjugate of the dominant FM signal; and a circuit to multiply said cross-products with the dominant FM signal to obtain a signal which contains all the original underlying signals without the dominant FM signal present.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is block diagram illustrating the basic concept underlying the invention.

FIG. 2 is a detailed functional block diagram of the preferred embodiment of the invention.

FIG. 3 is a detailed functional block diagram of an alternative embodiment of the cancellation circuit of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 illustrates the basic concept underlying the invention. The signal input **10** comprises a dominant FM signal along with any number of underlying signals. The underlying signals can be FM or some other modulation type. The FM demodulator **12** is captured by the dominant FM signal, and demodulates it. The demodulated signal **14** is then fed into an FM modulator **16** which uses demodulated signal **14** along with a delayed version of the signal input **22** to generate a high-fidelity replica **18** of the dominant FM signal within the signal input **10**. In cancellation circuit **26**, the replica **18** is used to remove the dominant signal from the delayed signal input **22**, leaving the underlying signal(s) **20** intact. The purpose of the delay **24** is to compensate for the time delay incurred in the FM demodulation process.

In the present invention as shown in FIG. **2**, FM demodulation is performed by phase-lock loop **100**. FM modulation is performed by phase-lock loop **200**. The cancellation process is performed by cancellation circuit **300**.

FIG. **2** illustrates the preferred embodiment of the invention comprising hard limiters **31** and **38**, delay **35**, low-pass filter **36**, amplifier **37**, phase-lock loops **100** and **200**, and cancellation circuit **300**. All of these devices could be implemented in analog hardware, digital hardware, DSP (Digital Signal Processing) software, or a combination of all three. For this reason, the following detailed description will focus upon the function of each element within the invention, rather than on the implementation.

Hard limiters **31** and **38** are for the purpose of enhancing the tracking performance of phase-lock loops **100** and **200**. Specifically, they improve phase-detector performance by removing all amplitude variations in the input.

Phase-lock loop (PLL) **100** performs FM demodulation of the dominant FM signal. It comprises phase detector **32**, loop filter **33**, and VCO **34**. The input is $V_2(t)$ containing the hard-limited dominant FM signal and underlying signal(s). The output is $V_4(t)$, containing the modulating signal driving the VCO. The design of PLL **100** is standard and can be realized with commercially available off-the-shelf components. However, performance is enhanced significantly by employing a wide-band type III loop (i.e. loop bandwidth greater than the RF bandwidth of the dominant FM signal, and loop filter containing two ideal integrators). To enhance performance further in certain applications, compensators could be designed into the loop as well.

Low-pass filter **36** averages $V_4(t)$ over time to produce $V_6(t)$, which is then amplified by amplifier **37** to create a clean replica of the signal modulating the dominant FM carrier signal. The averaging performed by the low-pass filter enhances the FM capture effect by removing the interference of the underlying signals upon the dominant FM signal. The gain of amplifier **37** should be set such that the voltage-frequency conversion gain from $V_4(t)$ to $V_{15}(t)$ is the same as that from $V_4(t)$ to $V_5(t)$.

Delay **35** compensates for the time delay through low-pass filter **36**, and is set to that value. In practice this delay

may be on the order of hundreds of microseconds, and would thus be difficult to implement at high carrier frequencies using analog circuitry. The preferred implementation employs an analog-digital approach, where $V_1(t)$ is A/D converted, docked into a FIFO buffer, and then D/A converted to form $V_8(t)$. The length of the buffer (and clock rate) determines the length of the delay. This implementation allows one to realize delays of several hundred microseconds with better than 100 nanosecond resolution. It is suitable for both analog and digital implementations of the invention.

PLL **200** creates a replica of the dominant FM signal present in $V_8(t)$. It comprises phase detector **39**, loop filter **40**, combiner **41**, and VCO **42**. The input is $V_9(t)$ containing the dominant FM signal and underlying signal(s) hard-limited and delayed in time. The output is $V_{13}(t)$, the output of the VCO **42**. The design of the PLL **200** is standard and can be realized with commercially available off-the-shelf components. However, for good performance it is critical that loop filter **40** be designed such that the overall loop bandwidth is very narrow (i.e. less than one-tenth the bandwidth of the signal modulating the dominant FM carrier). The narrow loop bandwidth of PLL **200** thus ensures that the average frequency of VCO output $V_{13}(t)$ is precisely equal to the average frequency of the dominant FM signal in $V_9(t)$. Adding $V_7(t)$ to the VCO input ensures that the instantaneous frequency of $V_{13}(t)$ equals that of the dominant FM signal in $V_9(t)$. The result is that the PLL **200** output, $V_{13}(t)$ is matched in frequency to the dominant FM signal in $V_8(t)$ and $V_9(t)$.

Cancellation circuit **300** comprises quadrature hybrids **43** and **44**, complex-conjugation circuit **45**, complex mixers **46** and **48**, and complex high-pass filter **47**. All of these functional elements can be implemented in analog circuitry with commercially available off-the-shelf parts, or using Digital Signal Processing (DSP), or a combination of the two.

The inputs to file cancellation circuit are $V_8(t)$ and $V_{13}(t)$. The former is the original signal input consisting of the dominant FM signal plus underlying signals, and the latter is a high-fidelity replica of the dominant FM signal in $V_8(t)$. The two inputs are each fed into two separate quadrature hybrids **43**, **44** which generate $V_{16}(t)$ and $V_{14}(t)$, complex signal representations of each of the inputs. $V_{15}(t)$ is the complex-conjugate of $V_{14}(t)$, and when it is multiplied with $V_{16}(t)$, the dominant FM signal is demodulated to a single spectral line at zero-frequency, $V_{17}(t)$. The high-pass filter **47** notches out this spectral line to produce $V_{18}(t)$. When $V_{18}(t)$ gets multiplied again (i.e. remodulated) with the dominant FM signal $V_{14}(t)$, the result is $V_{19}(t)$, which contains all the original underlying signal(s) without the dominant FM signal present. The underlying signal(s) can now be demodulated, or if necessary the next highest-power FM signal can be excised the same way the original dominant FM signal was excised by using an additional instance of the present invention connected in cascade.

A mathematical description of the theory underlying the cancellation circuit's operation is given below.

Let the dominant FM signal be denoted by D(t), the replica of the dominant signal be denoted by R(t), and fire combination of all the underlying signals be denoted by S(t). The original signal input is D(t)+S(t). Using complex exponentials, these signals can be represented as follows:

$$D(t)=|D|_e+(j\omega_D t+\phi)$$

$$S(t)=|S|_e+(j\omega_S t+\alpha)$$

$$R(t)=|R|_e+(j\omega_R t+\theta)$$

Note that if R(t), is a high-fidelity replica of D(t), then $\omega_R=\omega_D$. Thus, the first multiplication within the cancellation circuit gives:

$$[D(t)+S(t)]\cdot R^*(t) = [|D|e^{+(j\omega_D t+\phi)}+|S|e^{+(j\omega_S t+\alpha)}]\cdot|R|e^{-(j\omega_R t+\theta)} \quad (1)$$

$$= |D||R|e^{+j(\phi-\theta)}+|S||R|e^{+(j\omega_S t+\alpha)}e^{-(j\omega_R t+\theta)}$$

$$\text{High-pass filtering (1) yields: } = |S||R|e^{+(j\omega_S t+\alpha)}e^{-(j\omega_R t+\theta)} \quad (2)$$

Mutiplying (2) with the replica of the dominant FM signal, R(t), produces:

$$|S||R|_e+(j\omega_S t+\alpha)_e-(j\omega_R t+\theta)\cdot|R|_e+(j\omega_R t+\theta)=|S||R|^2_e+(j\omega_S t+\alpha) \quad (3)$$

Note that the dominant FM signal D(t), and the replica R(t) need not have equal magnitude nor equal phase (i.e. |D| need not equal |R|, and ϕ need not equal θ).

Complex representation of signals in the cancellation circuit as described above enables multiplication of signals without concern for spectral image-rejection. This is because the frequency spectra of complex signals are single-sided, and thus no spectral images are generated during the multiplication process. However, with proper design, complex representation of signals is not required.

An alternative embodiment of the cancellation circuit **300**, shown in FIG. **3**, uses conventional mixers **51**, **54**, **55** with only real (as opposed to complex) inputs. The high-pass filter **47** of the preferred embodiment is replaced by a notch-filter **50** centered at the frequency of a local oscillator **53**. Both the embodiments perform essentially the same function. Whereas the preferred embodiment demodulates the dominant FM signal to a single spectral line at zero-frequency before notching, the alternative embodiment described demodulates the dominant FM signal to a single spectral line at another particular frequency before notching. To obtain good performance with the alternative embodiment, one must exercise care in choosing the local oscillator frequency to avoid interference from spectral images. In either case, the notch should be made as narrow as possible.

The present invention solves the problems mentioned of the prior art by improving upon the invention(s) of Myers et al. in three important ways:

First, in this invention, the cancellation method employs a demodulation, notch-filtering, and remodulation process. The benefit of this method is that it does not require amplitude matching of the received dominant FM signal to the locally generated dominant FM signal replica. This cancellation method permits a fixed phase and/or small frequency offset between the received dominant FM signal and the replica as well.

Second, in Myers et at. U.S. Pat. No. 5,038.115, the primary function of the second phase-lock loop was to filter the output of the first phase-lock loop's VCO and add an additional 90° phase-shift in order to generate a 180° phase-shifted replica of the received dominant FM signal. In this invention, the second phase-lock loop **200** instead functions as an FM modulator. Namely, its purpose is to produce a high-fidelity replica (delayed in time) of the received dominant FM signal by using the output from the first phase-lock loop **100** as a modulating signal. The benefit of this is that it takes greater advantage of the FM capture-effect than the Myers et al. design, enabling generation of a very high-fidelity replica of the received dominant FM signal.

Third, the addition of a delay **35** to the inputs to the second phase-lock loop **200** and cancellation circuit **300** compensates for the delay through the low-pass filter **36** at

the output from the first phase-lock loop **100**. This delay is critical for ensuring that the second phase-lock loop **200** produces a high-fidelity replica of the received dominant FM signal. In also ensures that the input signals to the cancellation circuit **300** are time-aligned.

What is claimed is:

1. A device for removing a dominant FM signal from within a set of input signals occupying the same frequency band, comprising in combination:

a) FM demodulation means for recovering the modulating signal of a received dominant FM carrier signal;

b) FM modulation means for generating a replica of the received dominant FM carrier signal using the output of said FM demodulation means as the modulating signal;

c) delay means for aligning in time the original signal input to a replica of the dominant FM signal generated by said FM modulation means; and

d) cancellation means for removing the dominant FM signal from a set of input signals occupying the same frequency band;

said cancellation means comprising:

means to demodulate said dominant FM signal to a single spectral line;

means to filter out said spectral line to produce the cross-products of the dominant FM signal and underlying signals; and

means to multiply said signal cross-products with the dominant FM signal again to obtain a signal which contains all of the original underlying signal or signals without the dominant FM signal present.

* * * * *

US005826181A

United States Patent [19]

Reed

[11] Patent Number: 5,826,181

[45] Date of Patent: Oct. 20, 1998

[54] **RADIO FREQUENCY NOISE REDUCTION ARRANGEMENT**

[75] Inventor: **Christopher John Reed**, Harlow, Great Britain

[73] Assignee: **Northern Telecom Limited**, Montreal, Canada

[21] Appl. No.: **731,035**

[22] Filed: **Oct. 10, 1996**

[30] **Foreign Application Priority Data**

May 18, 1996 [GB] United Kingdom 9610498

[51] **Int. Cl.**[6] **H04B 1/10**

[52] **U.S. Cl.** **455/312**; 455/296; 455/280; 455/303; 455/304; 455/137; 329/336; 329/327

[58] **Field of Search** 455/312, 303, 455/304, 306, 296, 280, 137; 329/323, 325, 319, 320, 327, 336, 346

[56] **References Cited**

U.S. PATENT DOCUMENTS

3,480,867	11/1969	Sichak	455/304
4,027,264	5/1977	Gutleber	455/306
4,985,684	1/1991	Jentz et al.	329/327
5,548,838	8/1996	Talwar et al.	455/304

FOREIGN PATENT DOCUMENTS

2288038 10/1995 United Kingdom .

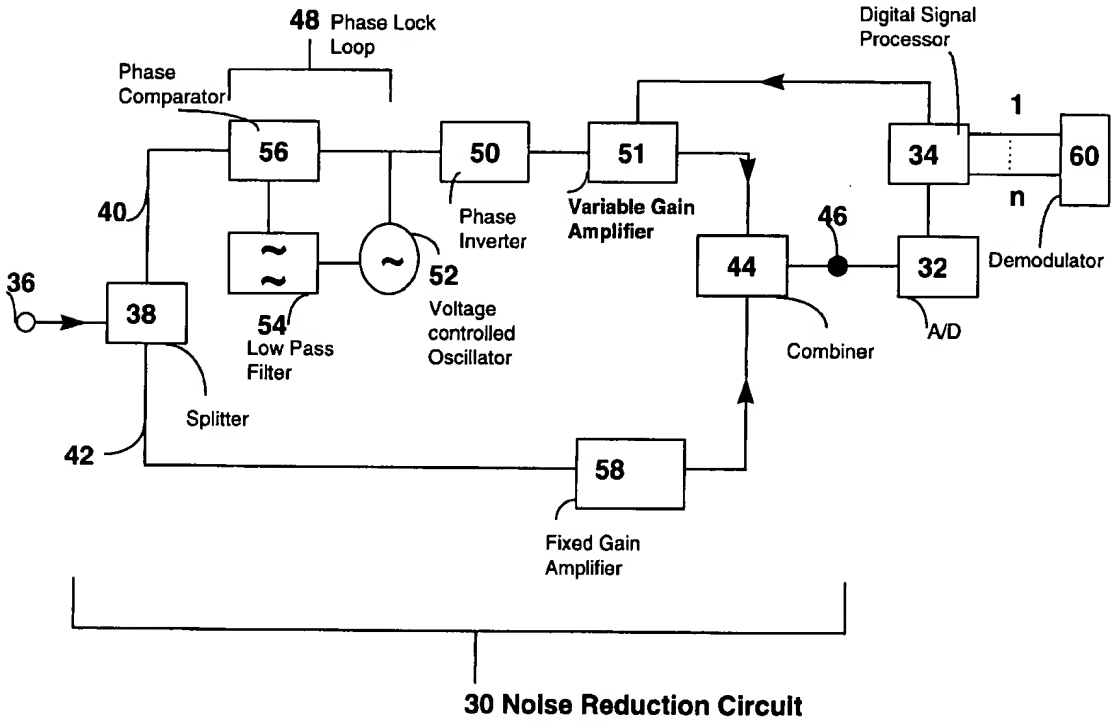
Primary Examiner—Donnie L. Crosland

Attorney, Agent, or Firm—John D. Crane

[57] **ABSTRACT**

A frequency selective noise reduction circuit and finds application in receiver demodulator arrangements in mobile telecommunication base stations. A receive signal is divided into two paths. One path includes a Phase Lock Loop circuit (PLL) which is employed to identify noise. The noise signal is inverted and then combined with the other signal.

8 Claims, 4 Drawing Sheets



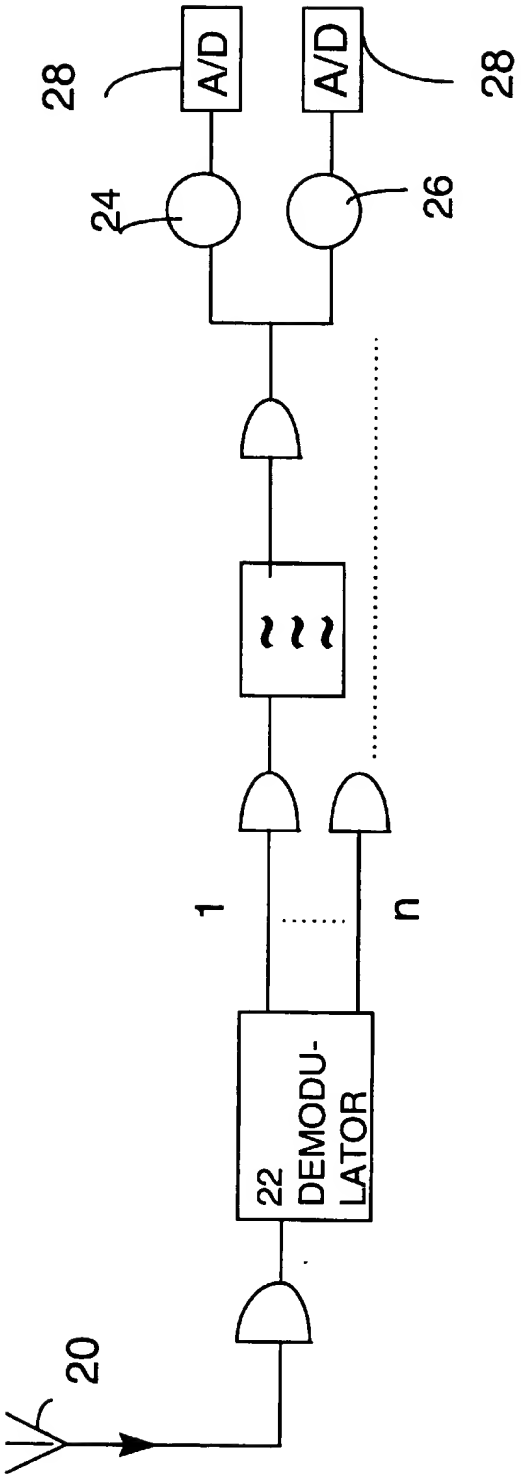


FIGURE 1

PRIOR ART

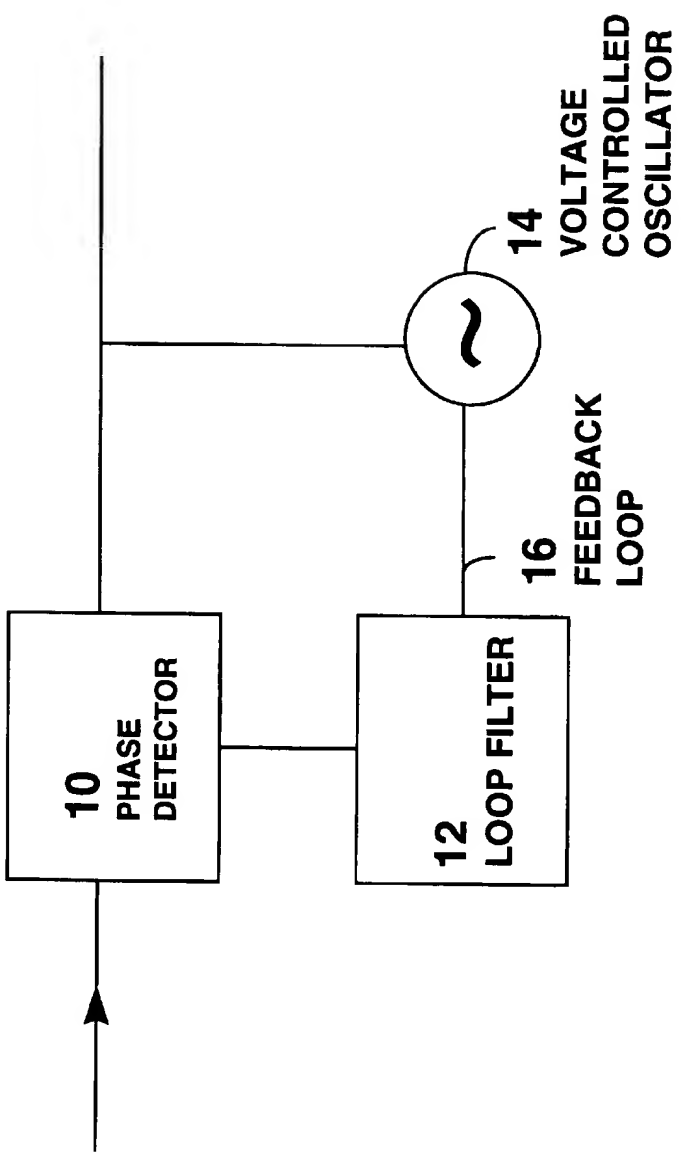

10
PHASE
DETECTOR
12
LOOP FILTER
16
FEEDBACK
LOOP
14
VOLTAGE
CONTROLLED
OSCILLATOR
prior art

FIGURE 2

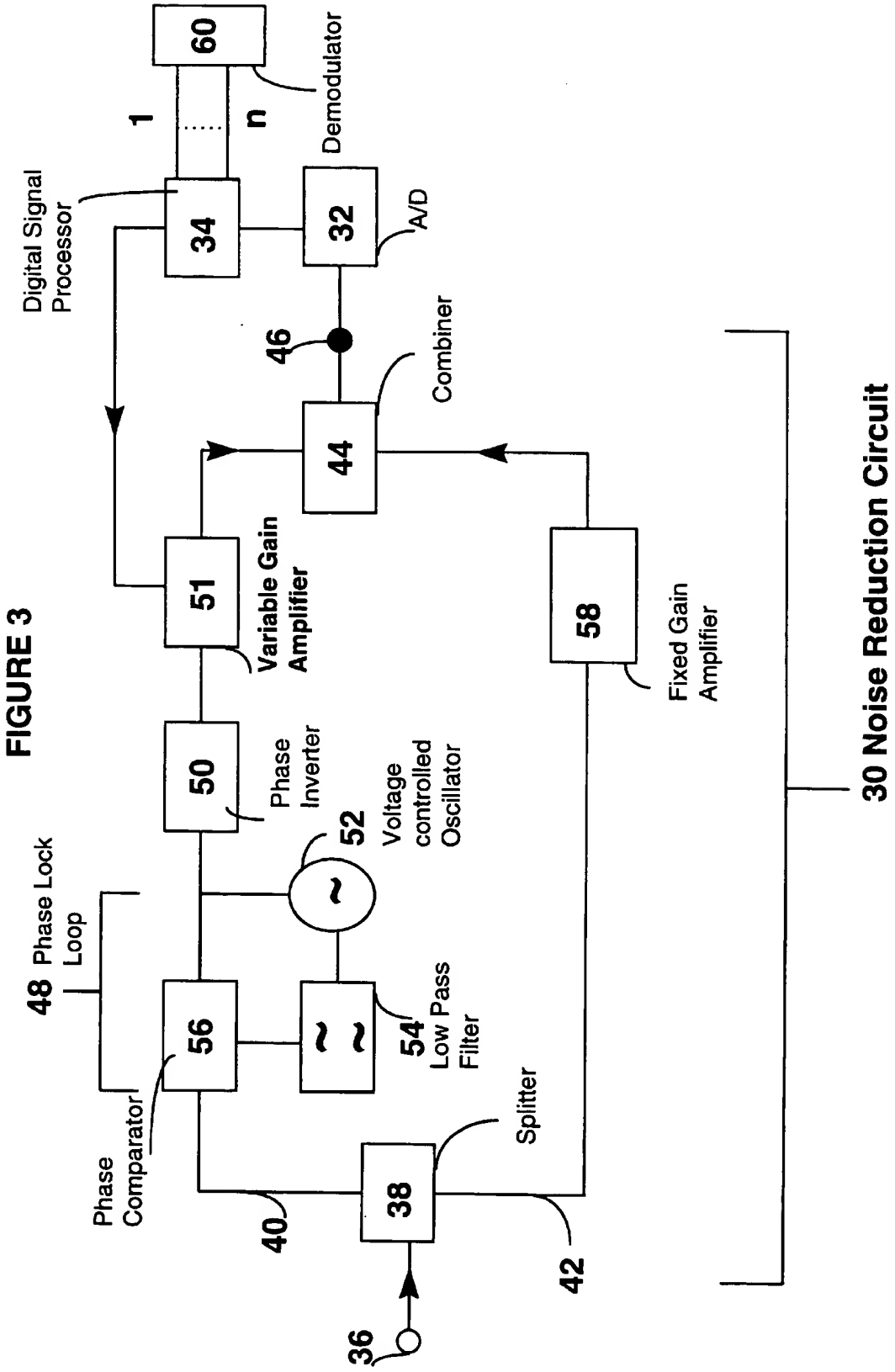

60
Demodulator
1
n
Digital Signal Processor
34
32
A/D
46
Combiner
44
51
Variable Gain Amplifier
58
Fixed Gain Amplifier
30 Noise Reduction Circuit
50
Phase Inverter
52
Voltage controlled Oscillator
48 Phase Lock Loop
56
54
Low Pass Filter
Phase Comparator
Splitter
38
40
42
36

FIGURE 3

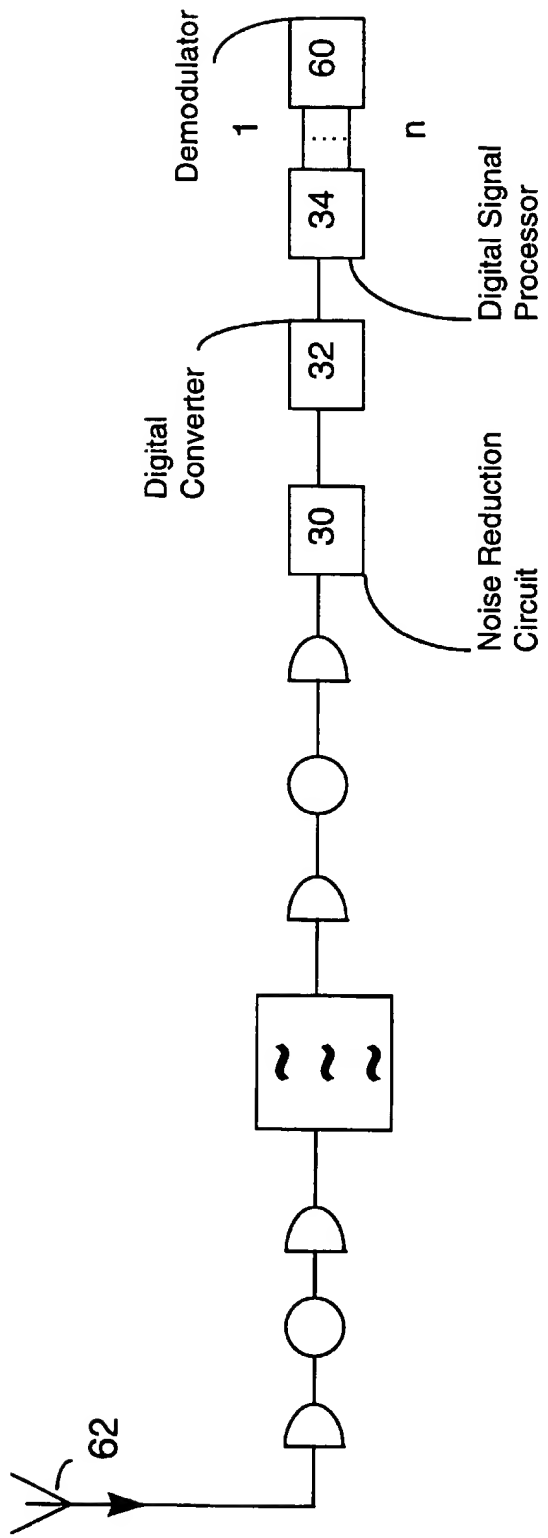

Demodulator
1
n
60
34
Digital Signal Processor
32
Digital Converter
30
Noise Reduction Circuit
62

FIGURE 4

RADIO FREQUENCY NOISE REDUCTION ARRANGEMENT

FIELD OF THE INVENTION

This invention relates to a frequency selective noise reduction arrangement operating at radio frequency and, in particular but not exclusively, relates to such an arrangement for use in a receiver in a wide-band cellular radio base station.

BACKGROUND TO THE INVENTION

In the field of mobile radio, wideband receivers have been proposed as a cost effective architecture for base stations. A single radio receiver and wideband analogue to digital converter (ADC) would digitise all signals simultaneously with a digital signal processor (DSP) performing the channel selection. Accordingly, a wide band receiver would need to be capable of simultaneously receiving weak signals from mobile stations at the edge of a cell and strong signals from mobile stations very close to the base station installation whilst distinguishing from normal transmissions to installations operated by competing operators and other sources of interference. In order to be so capable, a receiver needs to have an instantaneous spurious free dynamic range approaching 100 dB which current wideband ADCs do not meet. Signals received at an ADC in excess of the ADC full-scale level will prevent reception of all other signals.

A desirable characteristic of a receiver would be the ability to reduce the power of the strongest signal prior to demodulation, whose signal to noise ratio is much higher than is required for good reception, to a level so as to fall within the available dynamic range of the ADC without affecting the other signals within the band. Such an arrangement should be adaptive so that the system is flexible and fast in operation. Traditional noise cancellation arrangements tend to be frequency indiscriminate and as such are unsuitable for the above application. For the purposes of this description, a noise signal is one which is either too large for the dynamic range of the signal processing means of the base station or one produced by an interferer.

OBJECT OF THE INVENTION

Accordingly, it is an object of the present invention to provide an improved frequency selective noise reduction arrangement.

SUMMARY OF THE INVENTION

In accordance one aspect of the present invention, there is provided a frequency selective noise reduction arrangement operating at radio frequency comprising an input, a divider, a combiner, an output and first and second paths between the divider and combiner; wherein the first path possesses a phase lock loop circuit, an amplifier and a phase inverter and the second path is connected to the combiner; wherein the divider is operable to divide an input signal into the first and second paths and the first path is operable to select, amplify and phase invert a noise signal present in the input signal; wherein the combiner is operable to combine the signal of the first path with the signal of the second path; and wherein the phase inverted and amplified noise signal of the first path can be combined with the noise signal in the second path by the combiner whereby the noise is reduced from the output signal at the output of the combiner.

Preferably the amplifier in the first path is a variable amplifier or attenuator which is operable to vary the amplitude of the phase inverted signal whereby the noise in the first path is reduced. A power detector can be associated with the combiner as part of a feedback circuit to determine the extent of the amplification necessary in the variable amplifier. Alternatively, the feedback circuit can be associated with a detector in an associated analogue to digital converter. An amplifier or attenuator can also be provided in the second path which amplifier or attenuator may also be variable and controlled by a feedback loop. By the use of such an arrangement within, for example, a cellular radio base station, the need for a large number of mixers, amplifiers, filters and analogue to digital converters is conveniently avoided, since the noise reduction circuit can operate across all channels enabling a reduction in components, cost and size amongst other advantages.

In accordance with another aspect of the present arrangement, there is provided a method of operating a frequency selective noise reduction arrangement operating at radio frequency comprising an input, a divider, a combiner, first and second paths between the divider and an output; wherein, in the first path there is provided a phase lock loop circuit, an amplifier and a phase inverter and the second path is connected to the combiner; the method comprising the steps of dividing an input signal by means of the divider into the first and second paths; selecting, amplifying and phase inverting a noise signal present in the first path feeding the signal in the second path from the divider to the combiner; and combining the phase inverted and amplified signal from the first path with the signal in the second path by the combiner, whereby noise is reduced from the output signal.

The phase of the noise signal is thus inverted and then adaptively amplified by the variable gain amplifier; the phase locked loop (PLL) at an intermediate frequency (IF) replicates the dominant signal before adaptively reducing it.

In accordance with a further aspect of the invention, there is provided a method of receiving signals in a telecommunications base station receiver which includes a frequency selective noise reduction arrangement operating at radio frequency; which noise reduction arrangement comprises an input, a divider, a combiner, first and second paths between the divider and an output; wherein, in the first path there is provided a phase lock loop circuit, an amplifier and a phase inverter and the second path is connected to the combiner; the method comprising the steps of receiving signals from an antenna; passing the signals received from the antenna to the noise reduction arrangement, dividing the signal input to the noise reduction arrangement by means of the divider into the first and second paths; selecting, amplifying and phase inverting a noise signal present in the first path; feeding the signal in the second path from the divider to the combiner; combining the phase inverted and amplified signal from the first path with the signal in the second path by the combiner whereby noise is reduced from a signal output from the noise reduction arrangement; and feeding the output signal to an analogue to digital converter prior to further signal processing and demodulation.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be described with reference to the accompanying drawings, wherein:

FIG. 1 shows a conventional antenna receive path for a cellular radio base station;

FIG. 2 depicts a basic phase lock loop layout;

FIG. 3 shows an embodiment of the invention;

FIG. 4 shows a receivr path from a cellular base station antenna employing an embodiment of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

FIG. 1 shows a diagrammatic representation of a conventional antenna receive path as typically used in a cellular radio base station. Signals from the antenna **20** are fed to a demodulator **22** which separates the a number (n, where $n \leq 20$) of signals within each frequency band. The signals from the demodulator are then amplified, mixed to an intermediate frequency, passed through a band pass filter to select signals at the intermediate frequency, and amplified further before being passed to in-phase and quadrature mixers **24, 26** prior to the analogue-to-digital converters **28** where the analogue signals are converted to digital representation. Separate routes from the demodulator to the analogue-to-digital converters exist for all frequency bands which results in a complex design and costly implementation thereof.

Frequency selective arrangements are common and typically employ phase locked loop (PLL) circuits. The basic structure of a PLL is shown in FIG. 2. The main components consist of a phase detector **10**, a loop filter **12**, a voltage controlled oscillator **14** and a feed back loop **16** which typically incorporates a divider. The PLL compares an incoming signal, such as a clock signal, with its feedback clock. The difference between these two signals generates an error signal proportional to the gain of the phase detector, Kd, which error signal is applied to the loop filter. The loop filter typically consists of an active single pole-zero filter such as a standard Miller integrator, providing both high dc gain, which reduces input phase error (usually the gain of the filter, G is not less than 40 dB) and low frequency bandwidth. The output of this active filter adjusts a Voltage Controlled Oscillator (VCO) or a crystal VCO (VCXO) to lock the output signal to the input signal. The VCO however may have a centre frequency (f_o) at a much higher frequency (depending on system requirements) and, therefore, a divide down counter may be placed within the feedback path, which completes the loop.

Referring now to FIG. 3, there is shown one embodiment of the present invention. The noise reduction circuit **30** is operable in conjunction with a wide band analogue to digital converter **32** which outputs to a digital signal processing means **34**. The noise reduction circuit comprises an input at **36**, a splitter **38** which splits into a first path **40** and a second path **42**, a combiner **44** which combines the outputs of the first and second paths and an output at **46**. The first arm leads from the splitter to a phase lock loop **48**, wherefrom the signals pass to a phase inverter **50** through a variable gain amplifier **51** to arrive at the combiner **44**. The phase lock loop circuit comprises a voltage controlled oscillator **52** and a low-pass filter **54** acting on a phase comparator **56**. The variable gain amplifier receives a feedback control signal from the digital signal processor **34**. The second arm includes a fixed gain amplifier **58**.

In operation, an input signal, instead of being fed directly to an input of an analogue to digital converter after down conversion, is fed to an input **36** of a noise reduction circuit. The signal input to the circuit is split at splitter **38**. The signal of the first path passes from the splitter to the phase comparator which is set so that the phase lock loop locks with a constant phase relationship. The whole band of interest is fed into the reference of the phase lock loop whose loop bandwidth is wide enough to track the modulation index of the noise signal. The cut off frequency of the low pass filter **54** corresponds to the noise signal modulation deviation (which will be a known operating parameter). The phase comparator compares the phase of a periodic input signal against the phase of the voltage controlled oscillator: the output of the phase comparator is a measure of the phase difference between its two inputs. The difference voltage is then filtered by the loop filter **54** and applied to the voltage controlled oscillator **52**. The control voltage of the voltage controlled oscillator changes the frequency in a direction that reduces the phase difference between the input signal and the local oscillator.

In normal circumstances, when a phase lock loop is locked, the control voltage is such that the frequency of the voltage controlled oscillator is exactly equal to the frequency of the input signal. In the case of the use of a phase lock loop for the reduction of a dominant noise signal the noise signal is selected. The phase of the output is inverted by phase inverter **50** and then adaptively amplified by the variable gain amplifier **51**. The signal of the second path is passed from the splitter to a combiner **44** after amplification by amplification means **58**.

At the combiner, this signal is combined with the amplified input signal of the first arm. The amplifier enables both noise signals at the combiner **44** to be of the same order of magnitude, whereby the amplified noise signal of the first arm is cancelled by the phase inverted amplified noise signal in the second arm. The signal is passed from the output **46** to the wide band analogue to digital converter, through the digital down converter to a demodulator **60**.

The phase of the noise signal is thus inverted and then adaptively amplified by the variable gain amplifier; the phase locked loop (PLL) at an intermediate frequency (IF) replicates the dominant signal. The variable gain amplifier amplifies the inverted signal so that both noise signals input at the combiner are of the same order of magnitude, whereby the amplified noise signal of the second path is reduced by the phase inverted amplified noise signal in the first path. The noise level is reduced to an acceptable level: it need not necessarily be completely cancelled. The power of a strong signal, whose signal to noise ratio is much higher than is required for good reception, can be reduced to a level so as to fall within the available dynamic range of the ADC without affecting the other signals within the band. Problems experienced with previous systems in overload situations where the desired signal is too strong and the analogue to digital converter operates in a non-linear mode can thus be prevented.

Perturbation would be suitable for the control algorithm; the power detection could be carried out within the digital signal processor, after the analogue to digital conversion or by measurement of the analogue signal applied to the analogue to digital converter. The output of the phase lock loop could be disabled when noise reduction is not required. Since the noise reduced signal may itself be demodulated, full noise reduction is not desirable. Alternative feedback means to the variable gain amplifier **51** (or attenuator) may be employed to one originating in the digital signal processing means **34**. For instance sensors may be present in the combiner.

FIG. 4 shows an arrangement in accordance with the present invention corresponding to the conventional arrangement shown in FIG. 2. Signals from an antenna **62** are passed through various amplifiers, mixers and filters to the noise reduction circuit where noise reduction can be performed before the conversion of signals to digital representation and demodulation. The multiplication (multiplication factor=n) of mixers, amplifiers, filters and analogue to digital converters is conveniently avoided,

enabling a reduction in components, cost and size amongst other advantages.

The use of the loop filter (54) within a PLL may require an unreasonable amount of time to provide a locked output clock. This problem may be overcome by increasing the PLL jitter bandwidth to provide a rapid lock-in time. Once in lock, the PLL would revert to its intended noise modulation deviation bandwidth.

The above approach will work for constant envelope signals only (FM, FSK, GMSK etc.) and when one signal is significantly more powerful than the average. Both of the above will be satisfied for AMPS and GSM.

I claim:

1. A frequency selective noise reduction arrangement operating at radio frequency comprising

an input, a divider, a combiner, an output and first and second paths between the divider and combiner;

wherein the first path possesses a phase lock loop circuit, an amplifier and a phase inverter and the second path is connected to the combiner;

wherein the divider is operable to divide an input signal into the first and second paths and the first path is operable to select, amplify and phase invert a noise signal present in the input signal;

wherein the combiner is operable to combine the signal of the first path with the signal of the second path; and

wherein the phase inverted and amplified noise signal of the first path can be combined with the noise signal in the second path by the combiner whereby the noise is reduced from the output signal at the output of the combiner.

2. An arrangement according to claim 1 wherein the amplifier in the first path is a variable amplifier which is operable to vary the amplitude of the phase inverted signal.

3. An arrangement according to claim 1 including a power detector associated with the combiner in a feedback loop and wherein the amplifier in the first path is a variable amplifier which is operable to vary the amplitude of the phase inverted signal, wherein the variable amplifier is controlled by the feedback loop.

4. A frequency selective noise reduction arrangement operating at radio frequency comprising

an input, a divider, a combiner, an output and first and second paths between the divider and combiner;

wherein the first path possesses a phase lock loop circuit, an amplifier and a phase inverter and the second path is connected to the combiner;

wherein the divider is operable to divide an input signal into the first and second paths and the first path is operable to select, amplify and phase invert a noise signal present in the input signal;

wherein the combiner is operable to combine the signal of the first path with the signal of the second path;

wherein the phase inverted and amplified noise signal of the first path can be combined with the noise signal in the second path by the combiner whereby the noise is reduced from the output signal at the output of the combiner; and

wherein there is an amplifier in the second path.

5. An arrangement according to claim 4 wherein the amplifier in the first path is a variable amplifier which is operable to vary the amplitude of the phase inverted signal, and wherein the amplifier in the second path is a variable amplifier and wherein there is a power detector associated with the combiner in a feedback loop, wherein the amplifier in the second path is controlled by the feedback loop.

6. A telecommunications base station receiver incorporating an arrangement according to claim 1.

7. A method of operating a frequency selective noise reduction arrangement operating at radio frequency comprising

an input, a divider, a combiner, first and second paths between the divider and an output;

wherein, in the first path there is provided a phase lock loop circuit, an amplifier and a phase inverter and the second path is connected to the combiner;

the method comprising the steps of dividing an input signal by means of the divider into the first and second paths;

selecting, amplifying and phase inverting a noise signal present in the first path feeding the signal in the second path from the divider to the combiner; and

combining the phase inverted and amplified signal from the first path with the signal in the second path by the combiner whereby noise is reduced from the output signal.

8. A method of receiving signals in a telecommunications base station receiver which includes a frequency selective noise reduction arrangement operating at radio frequency; which noise reduction arrangement comprises

an input, a divider, a combiner, first and second paths between the divider and an output;

wherein, in the first path there is provided a phase lock loop circuit, an amplifier and a phase inverter and the second path is connected to the combiner;

the method comprising the steps of receiving signals from an antenna;

passing the signals received from the antenna to the noise reduction arrangement, dividing the signal input to the noise reduction arrangement by means of the divider into the first and second paths;

selecting, amplifying and phase inverting a noise signal present in the first path;

feeding the signal in the second path from the divider to the combiner;

combining the phase inverted and amplified signal from the first path with the signal in the second path by the combiner whereby noise is reduced from a signal output from the noise reduction arrangement; and

feeding the output signal to an analogue to digital converter prior to further signal processing and demodulation.

* * * * *